List of Publications of Pramod Kumar Meher

ABSTRACT

(A) Recently Accepted Papers

1. S. M. Cho, **P. K. Meher**, L. T. N.Trung, H. J. Cho, and S. Y. Park, 'Design of Very High-Speed Pipeline FIR Filter Through Precise Critical Path Analysis', *Accepted for publication IEEE Access*, Impact Factor: 3.745.

2. P. Mishra, A. Banerjee, M. Ghosh, S. Gogoi, and **P. K. Meher**, 'Implementation and Validation of Quadral-Duty Digital PWM to Develop a Cost-optimized ASIC for BLDC Motor Drive,' *Accepted for publication in Elsevier Journal of Control Engineering Practice*, Impact Factor: 3.193.

3. **P. K. Meher**, S-K. Lam, T. Srikanthan, D. H. Kim, S. Y. Park 'Area-Time Efficient 2-Dimensional Reconfigurable Integer DCT Architecture for HEVC,' *Accepted for publication in MDPI Journal of Electronics,*, Impact Factor 2.412..

(B) Books and Book Chapters

1. 'Arithmetic Circuits for DSP Applications' Edited by **P. K. Meher** and T. Stouraitis, Wiley-IEEE Press, ISBN: 978-1-119-20677-4, 2017.

2. S. B. Jdidia, Maher Jridi, **P. K. Meher**, N. Masmoudi, and A. AlFalou, 'Scalable Transform Architectures for Video Coding,' Chapter-1, *in VLSI Architectures for Future Video Coding*, Institution of Engineering & Technology Publication, pp.1-39, November, 2019.

3. **P. K. Meher**, C.-H. Chang, O. Gustafsson, A.P. Vinod, and M. Faust, 'Shift-Add Circuits for Constant Multiplications,' Chapter-2, *in Arithmetic Circuits for DSP Applications*, Wiley-IEEE Press, pp.33-77, September, 2017.

4. M. Mehendale, M. Sharma, and **P. K. Meher**, 'DA-Based Circuits for Inner-Product Computation,' Chapter-3, *in Arithmetic Circuits for DSP Applications*, Wiley-IEEE Press, pp.78-113, September, 2017.

5. **P. K. Meher** and S-F. Hsiao, 'Table-based Circuits for DSP Applications,' Chapter-4, *in Arithmetic Circuits for DSP Applications*, Wiley-IEEE Press, pp.114-149, September, 2017.

6. **P. K. Meher**, J. Valls, T-B. Juang, K. Sridharan, and K. Maharatna, 'CORDIC Circuits,' Chapter-5, *in Arithmetic Circuits for DSP Applications*, Wiley-IEEE Press, pp.150-186, September, 2017.

7. **P. K. Meher**, 'Systolic VLSI and FPGA Realization of Artificial Neural Networks,' *in Computational Intelligence in Optimization*, Springer-Verlag, Berlin Heidelberg, pp.359-380, 2010.

8. C-Y. Lee, **P. K. Meher**, C. W. Chiou, and J-M. Lin, 'Concurrent Error Detection/Correction in Finite Field Arithmetic Architectures over GF(2^m),' *in Cryptography Research Perspectives*, NOVA Publisher, pp.49-96, New York 2010.

(C) JOURNAL PUBLICATIONS

(IEEE Publications are listed first, followed by IEE/IET and other Publications.)

1. B.K. Mohanty and **P. K. Meher**, 'An Efficient Parallel DA-based Fixed-Width Design for Approximate Inner-Product Computation,' *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 5, pp. 1221-1229, May 2020.

2. D. Ray, N. V. George, **P. K. Meher**, 'Analysis and Design of Unified Architectures for Zero-Attraction-Based Sparse Adaptive Filters,' *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 28, no. 5, pp. 1321-1325, May 2020.

3. D. Ray, N. V. George, and **P. K. Meher**, 'An Analytical Framework and Approximation Strategy for Efficient Implementation of Distributed Arithmetic-Based Inner-Product Architectures,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 1, pp. 212-224, Jan. 2020.

4. Jiafeng Xie, C-Y. Lee, **P. K. Meher**, and Zhi-Hong Mao, 'Novel Bit-Parallel and Digit-Serial Systolic Finite Field Multipliers over $GF(2^m)$ based on Reordered Normal Basis,' *IEEE Transactions on Very Large Scale Integration Systems*, vol.27, no.9, pp.2119-2130, September 2019.

5. S. K. Sahoo, **P. K. Meher**, and G Ganesh Kumar, 'Multichannel Filters for Wireless Networks: Lookup-Table-Based Efficient Implementation,' *IEEE Consumer Electronics Magazine*, vol.8, no.3, pp. 44-49, May 2019.

6. B.K. Mohanty and **P. K. Meher**, 'Area-Delay-Energy Efficient VLSI Architecture for Scalable In-place Computation of FFT on Real Data,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.66, no.3, pp.1042-1050, March 2019.

7. B. A. Jasani, S-K. Lam, **P. K. Meher**, and M. Wu, 'Threshold-Guided Design and Optimization for Harris Corner Detector Architecture,' *IEEE Transactions on Circuits and Systems for Video Technology*, vol.28, no.12, pp.3516-3526, December 2018.

8. Dwaipayan Ray, Nithin George, and **P. K. Meher**, 'Efficient Shift-Add Implementation of FIR Filters using Variable Partition Hybrid Form Structures,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.65, no.12, pp.4247-4257, December 2018.

9. Jiafeng Xie, **P. K. Meher**, X. Zhou, and C-Y. Lee, 'Low Register-Complexity Systolic Digit-Serial Multiplier over $GF(2^m)$ based on Trinomials,' *IIEEE Transactions on on Multi-Scale Computing Systems*, vol.4, no.4, pp.773-783, Oct-Dec 2018.

10. Xin Lou, **P. K. Meher**, Ya Jun Yu, and Ye Wenbin, 'Novel Structure for Area-Efficient Implementation of FIR Filter,' *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol.64, no.10, pp.1212-1216, October 2017.

11. Maher Jridi and **P. K. Meher**, 'A Scalable Approximate DCT Architectures for Efficient HEVC Compliant Video Coding,' *IEEE Transactions on Circuits and Systems for Video Technology*, vol.27, no.8, pp.1815-1825, August 2017.

12. Jiafeng Xie, **P. K. Meher**, Mingui Sun, Yuecheng Li, Bo Zeng, and Zhi-Hong Mao, 'Efficient FPGA Implementation of Low-Complexity Systolic Karatsuba Multiplier over GF(2^m) Based on NIST Polynomials,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.64, no.7, pp.1815-1825, March 2017.

13. Xin Lou, Ya Jun Yu, and **P. K. Meher**, 'Lower Bound Analysis and Perturbation of Critical Path for Area-Time Efficient Multiple Constant Multiplications,' *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol.36, no.2, pp.313-324, February 2017.

14. **P. K. Meher** and Xin Lou, 'Low-Latency, Low-Area, and Scalable Systolic-Like Modular Multipliers for $GF(2^m)$ Based on Irreducible All-One Polynomials,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.64, no.2, pp.399-408, February 2017.

15. C-Y. Lee, **P. K. Meher**, C-C. Fan, and S-M. Yuan 'Low-Complexity Digit-Serial Multiplier over GF(2^m) based on Efficient Toeplitz Block Toepliz Matrix-Vector Product Decomposition,' *IEEE Transactions on VLSI Systems*, vol.25, no.2, pp.735-746, February 2017.

16. Xin Lou, Ya Jun Yu, and **P. K. Meher**, 'Analysis and Optimization of Product-Accumulation Section for Efficient Implementation of FIR Filters,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.63, no.10, pp.1701-1713, October 2016.

17. C-Y. Lee and **P. K. Meher** 'Comment on "Subquadratic Space-Complexity Digit-Serial Multipliers Over GF(2^m) Using Generalized (a, b)-Way Karatsuba Algorithm,' *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol.63, no.8, pp.1316-1319, August 2016.

18. C-Y. Lee, **P. K. Meher**, and C-H Liu 'Area-Delay Efficient Digit-Serial Multiplier Based on k-Partitioning Scheme Combined with TMVP Block Recombination Approach,' *IEEE Transactions on VLSI Systems*, vol.24, no.7, pp.2413-2425, July 2016.

19. B. K. Mohanty, **P. K. Meher**, and S. Patel, 'LUT Optimization for Distributed Arithmetic-Based Block Least Mean Square Adaptive Filter,' *IEEE Transactions on VLSI Systems*, vol.24, no.5, pp.1926-1935, May 2016.

20. **P. K. Meher**, 'On Efficient Retiming of Fixed-Point Circuits,' *IEEE Transactions on VLSI Systems*, vol.24, no.4, pp.1257-1265, April 2016.

21. S. Aggarwal, **P. K. Meher**, and K. Khare, 'Concept, Design, and Implementation of Reconfigurable CORDIC,' *IEEE Transactions on VLSI Systems*, vol.24, no.4, pp.1588-1592, April 2016.

22. B. K. Mohanty and **P. K. Meher**, 'A High-Performance FIR Filter Architecture for Fixed and Reconfigurable Applications,' *IEEE Transactions on VLSI Systems*, vol.24, no.2, pp.444-452, February 2016.

23. **P. K. Meher**, B. K. Mohanty, S. Patel, S. Ganguly, and T. Srikanthan, 'Efficient VLSI Architecture for Decimation-in-Time Fast Fourier Transform of Real-Valued Data,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.12, pp.2836-2845, December 2015.

24. C-Y. Lee and **P. K. Meher**, 'Area-Efficient Subquadratic Space-Complexity Digit-Serial Multiplier for Type-II Optimal Normal Basis of $GF(2^m)$ using Symmetric TMVP and Block Recombination Techniques,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.12, pp.2846-2855, December 2015.

25. Xin Lou, Ya Jun Yu, and **P. K. Meher**, 'New Approach to the Reduction of Sign-Extension Overhead for Efficient Implementation of Multiple Constant Multiplications,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.11, pp.2695-2705, November 2015.

26. H. Rabah, A. Amira, B. K. Mohanty, S. Al-Maadeed, and **P. K. Meher**, 'FPGA Implementation of Orthogonal Matching Pursuit for Compressive Sensing Reconstruction,' *IEEE Transactions on VLSI Systems*, vol.23, no.10, pp.2209-2220, October 2015.

27. C-H Liu, C-Y. Lee, and **P. K. Meher**, 'Efficient Digit-Serial KA-based Multiplier over Binary Extension Fields using Block Recombination Approach,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.8, pp.2044-2051, August 2015.

28. S-F. Hsiao, P-H. Wu, C-S. Wen, and **P. K. Meher**, 'Table-Size Reduction Methods for Faithfully-Rounded Lookup-Table-Based Multiplierless Function Evaluation,' *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol.62, no.5, pp.466-470, May 2015.

29. Jiafeng Xie, **P. K. Meher** and Zhi-Hong Mao, 'High-Throughput Digit-Level Systolic Multiplier over GF(2^m) Based on Irreducible Trinomials,' *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol.62, no.5, pp.481-485, May 2015.

30. C-Y. Lee and **P. K. Meher**, 'Subquadratic Space-Complexity Digit-Serial Multipliers over $GF(2^m)$ using Generalized (a, b)-way Karatsuba Algorithm,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.4, pp.1091-1098, April 2015.

31. Jiafeng Xie, **P. K. Meher** and Zhi-Hong Mao, 'Low-Latency High-Throughput Systolic Multipliers over GF(2^m) for NIST Recommended Pentanomials,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.3, pp.881-890, March 2015.

32. Xin Lou, Ya Jun Yu, and **P. K. Meher**, 'Fine-Grained Critical Path Analysis and Optimization for Area-Time Efficient Realization of Multiple Constant Multiplications,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.3, pp.863-872, March 2015.

33. C-Y. Lee and **P. K. Meher**, 'Efficient Subquadratic Space Complexity Architectures for Parallel MPB Single- and Double-Multiplications for All Trinomials Using Toeplitz Matrix-Vector Product Decomposition,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.3, pp.854-862, March 2015.

34. Maher Jridi, Ayman Alfalou, and **P. K. Meher**, 'A Generalized Algorithm and Reconfigurable Architecture for Efficient and Scalable Orthogonal Approximation of DCT,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.2, pp.449-457, February 2015.

35. Jiafeng Xie, **P. K. Meher** and Zhi-Hong Mao, 'High-Throughput Finite Field Multipliers using Redundant Basis for FPGA and ASIC Implementations,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.62, no.1, pp.110-119, January 2015.

36. C-Y. Lee, **P. K. Meher** and C-P. Chang, 'Efficient M-ary Exponentiation over GF(2^m) using Subquadratic KA-Based Three-Operand Montgomery Multiplier,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.61, no.11, pp.3125-3134, November 2014.

37. C-Y. Lee, C-S. Yang, B. K. Meher, **P. K. Meher**, and J-S. Pan, 'Low-Complexity Digit-Serial and Scalable SPB/GPB Multipliers over Large Binary Extension Fields using (b,2)-Way Karatsuba Decomposition,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.61, no.11, pp.3115-3124, November 2014.

38. S. Y. Park and **P. K. Meher**, 'Efficient FPGA and ASIC Realizations of DA-Based Reconfigurable FIR Digital Filter,' *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol.61, no.7, pp.511-515, July 2014.

39. **P. K. Meher** and S. Y. Park, 'Critical-Path Analysis and Low-Complexity Implementation of the LMS Adaptive Algorithm,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.61, no.3, pp.778-788, March 2014.

40. Y. Pan and **P. K. Meher**, 'Bit-Level Optimization of Adder-Trees for Multiple Constant Multiplications for Efficient FIR Filter Implementation,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.61, no.2, pp.455-462, February 2014.

41. **P. K. Meher** and S. Y. Park, 'Area-Delay-Power Efficient Fixed-Point LMS Adaptive Filter with Low Adaptation-Delay,' *IEEE Transactions on VLSI Systems*, vol.22, no.2, pp.362-371, February 2014.

42. **P. K. Meher**, S. Y. Park, B. K. Mohanty, K. S. Lim, and C. H. Yeo, 'Efficient Integer DCT Architectures for HEVC,' *IEEE Transactions on Circuits & Systems for Video Technology*, vol.24, no.1, pp.168-178 , January 2014.

43. B. K. Mohanty, **P. K. Meher**, S. Al-Maadeed, and A. Amira, 'Memory Footprint Reduction for Power-Efficient Realization of 2-D Finite Impulse Response Filters,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.61, no.1, pp.120-133, January 2014.

44. J-S. Pan, C-Y. Lee, **P. K. Meher**, 'Low-Latency Digit-Serial and Digit-Parallel Systolic Multipliers for Large Binary Extension Fields,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.60, no.12, pp.3195-3204, December 2013.

45. S. Y. Park and **P. K. Meher**, 'Low-Power, High-Throughput, and Low-Area Adaptive FIR Filter Based on Distributed Arithmetic,' *IEEE Transactions on Circuits and Systems-II: Express Briefs*, vol.60, no.6, pp.346-350, June 2013.

46. Jiafeng Xie, **P. K. Meher**, and Jianjun He, 'Hardware-Efficient Realization of Prime-Length DCT Based on Distributed Arithmetic,' *IEEE Transactions on Computers*, vol.62, no.6, pp.1170-1178, June 2013.

47. B. K. Mohanty and **P. K. Meher**, 'A High-Performance Energy-Efficient Architecture for FIR Adaptive Filter based on New Distributed Arithmetic Formulation of Block LMS Algorithm,' *IEEE Transactions on Signal Processing*, vol.61, no.4, pp.921-932, April 2013.

48. B. K. Mohanty and **P. K. Meher**, 'Memory-Efficient High-Speed Convolution-Based Generic Structure for Multilevel 2-D DWT,' *IEEE Transactions on Circuits & Systems for Video Technology*, vol.23, no.2, pp.353-363, February 2013.

49. S. Aggarwal, **P. K. Meher** and K. Khare, 'Scale-Free Hyperbolic CORDIC Processor and its Application to Waveform Generation,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.60, no.2, pp.314-326, February 2013.

50. **P. K. Meher** and S. Y. Park, 'CORDIC Designs for Fixed Angle of Rotation,' *IEEE Transactions on VLSI Systems*, vol.21, no.2, pp.217-228, February 2013.

51. Jiafeng Xie, Jianjun He, and **P. K. Meher**, 'Low Latency Systolic Montgomery Multiplier for Finite Field GF(2^m) Based on Pentanomials,' *IEEE Transactions on VLSI Systems*, vol.21, no.2, pp.385-389, February 2013.

52. Jiafeng Xie, **P. K. Meher**, and Jianjun He, 'Low-Complexity Multiplier for GF(2^m) Based on All-One Polynomials,' *IEEE Transactions on VLSI Systems*, vol.21, no.1, pp.168-173, January 2013.

53. S. Aggarwal, **P. K. Meher**, and K. Khare, 'Area-Time Efficient Scaling-Free CORDIC using Generalized Micro-Rotation Selection,' *IEEE Transactions on VLSI Systems*, vol.20, no.8, pp.1542-1546, August 2012.

54. B. K. Mohanty, A. Mahajan, and **P. K. Meher**, 'Area and Power-Efficient Architecture for High-Throughput Implementation of Lifting 2-D DWT,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.59, no.7, pp.434-438, July 2012.

55. F. Garcia-Herrero, M. J. Canet, J. Valls and **P. K. Meher**, 'High-Throughput Interpolator Architecture for Low-Complexity Chase Decoding of RS Codes,' *IEEE Transactions on VLSI Systems*, vol.20, no.3, pp.568-573, March 2012.

56. B. K. Mohanty and **P. K. Meher**, 'Memory-Efficient Architecture for 3-D DWT Using Overlapped

Grouping of Frames,' *IEEE Transactions on Signal Processing*, vol.59, no.11, pp. 5605-5616, November 2011.

57. N. Sudha, A.R. Mohan, and **P. K. Meher**, 'A Self-Configurable Systolic Architecture for Face Recognition Based on Principal Component Neural Network,' *IEEE Transactions on Circuits & Systems for Video Technology*, vol.21, no.8, pp.1071-1084, August 2011.

58. B. K. Mohanty and **P. K. Meher**, 'Memory Efficient Modular VLSI Architecture for High-Throughput and Low-Latency Implementation of Multilevel Lifting 2-D DWT,' *IEEE Transactions on Signal Processing*, vol.59, no.5, pp.2072-2084, May 2011.

59. J. C. Patra, **P. K. Meher**, G. Chakraborty, 'Development of Laguerre Neural-Network-Based Intelligent Sensors for Wireless Sensor Networks,' *IEEE Transactions on Instrumentation & Measurement*, vol.60, no.3, pp.725-734, March 2011.

60. B. K. Mohanty and **P. K. Meher**, 'Parallel and Pipeline Architectures for High-Throughput Computation of Multilevel 3-D DWT,' *IEEE Trans. on Circuits & Systems for Video Technology*, vol.20, no.9, pp.1200-1209, September 2010.

61. C-Y Lee and **P. K. Meher**, 'Concurrent Error Detection in Bit-serial Normal Basis Multiplication over GF(2^m) using Multiple Parity Prediction Schemes,' *IEEE Transactions on VLSI Systems*, vol.18, no.8, pp.1234-1238, August 2010.

62. **P. K. Meher**, 'LUT Optimization for Memory-Based Computation,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.57, no.4, pp.285-289, April 2010.

63. **P. K. Meher**, 'New Approach to Look-up-Table Design and Memory-Based Realization of FIR Digital Filter,' *IEEE Transactions on Circuits & Systems-I: Regular Papers*, vol.57, no. 3, pp.592-603, March 2010.

64. L. Vachhani, K. Sridharan, and **P. K. Meher**, 'Efficient FPGA Realization of CORDIC with Application to Robotic Exploration,' *IEEE Transactions on Transactions on Industrial Electronics*, vol.56, no.12, pp.4915-4929, December 2009.

65. **P. K. Meher**, J. Valls, T-B Juang, K. Sridharan, and K. Maharatna, '50 Years of CORDIC: Algorithms, Architectures and Applications,' *IEEE Transactions on Circuits & Systems-I: Regular Papers*, vol.56, no.9, pp.1893- 1907, September 2009.

66. **P. K. Meher**, 'Systolic and Non-systolic Scalable Modular Designs of Finite Field Multipliers for Reed-Solomon Codec,' *IIEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.17, no.6, pp.747-757, June 2009.

67. **P. K. Meher**, 'On Efficient Implementation of Accumulation in Finite Field over GF(2^m) and its Applications,' *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol.17, no.4, pp.541-550, April 2009.

68. **P. K. Meher**, 'Extended Sequential Logic for Synchronous Circuit Optimization and Its Applications,' *IEEE Transactions Computer-Aided Design of Integrated Circuits and Systems*, vol.28, no.4, pp.469-477, April 2009.

69. L. Vachhani, K. Sridharan, and **P. K. Meher**, 'Efficient CORDIC Algorithms and Architectures for Low Area and High Throughput Implementation,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.56, no.1, pp.61- 65, January 2009.

70. **P. K. Meher**, 'Parallel and Pipelined Architectures for Cyclic Convolution by Block Circulant Formulation using Low-Complexity Short-Length Algorithms,' *IEEE Transactions on Circuits & Systems*

for Video Technology, vol.18, no.10, pp.1422-1431, October 2008.

71. **P. K. Meher**, 'New Approach to Scalable Parallel and Pipelined Realization of Repetitive Multiple-Accumulations,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.55, no.9, pp.902-906, September 2008.

72. **P. K. Meher**, S. Chandrasekaran, and A. Amira, 'FPGA Realization of FIR Filters by Efficient and Flexible Systolization Using Distributed Arithmetic,' *IEEE Transactions on Signal Processing*, vol.56, no.7, pp.3009-3017, July 2008.

73. J. C. Patra, G. Chakraborty, and **P. K. Meher**, 'Neural Network-Based Robust Linearization and Compensation Technique for Sensors under Nonlinear Environmental Influences,' *IEEE Transactions on Circuits and Systems-I: Regular Papers*, vol.55, no.5, pp.1316-1327, May 2008.

74. **P. K. Meher**, 'Systolic and Super-Systolic Multipliers for Finite Field GF(2^m) Based on Irreducible Trinomials,' *IEEE Transactions on Circuits & Systems-I: Regular Papers*, vol.55, no.4, pp.1031-1040, April 2008.

75. **P. K. Meher**, B. K. Mohanty and J. C. Patra, 'Hardware-Efficient Systolic-Like Modular Design for Two-Dimensional Discrete Wavelet Transform,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.55, no.2, pp.151-155, February 2008.

76. **P. K. Meher**, J. C. Patra and M. N. S. Swamy, 'High-Throughput Memory-Based Architecture for DHT Using a New Convolutional Formulation,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.54, no.7, pp.606-610, July 2007.

77. **P. K. Meher** and M. N. S. Swamy, 'New Systolic Algorithm and Array Architecture for Prime-Length Discrete Sine Transform,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.54, no.2, pp.262-266, March 2007.

78. **P. K. Meher**, 'Unified Systolic-Like Architecture for DCT and DST Using Distributed Arithmetic,' *IEEE Transactions on Circuits & Systems-I: Regular Papers*, vol.53, no.12, pp.2656-2663, December 2006.

79. **P. K. Meher**, 'Systolic Designs for DCT using a Low-Complexity Concurrent Convolutional Formulation,' *IEEE Trans. on Circuits & Systems for Video Technology*, vol.16, no.9, pp.1041-1050, September 2006.

80. **P. K. Meher**, 'Hardware-Efficient Systolization of DA-based Calculation of Finite Digital Convolution,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.53, no.8, pp.707-711, August 2006.

81. **P. K. Meher**, 'Efficient Systolic Implementation of DFT using a Low-Complexity Convolution-Like Formulation,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.53, no.8, pp.702-706, August 2006.

82. **P. K. Meher**, 'Highly Concurrent Reduced-Complexity 2-D Systolic Array for Discrete Fourier Transform,' *IEEE Signal Processing Letters*, vol.13, no.8, pp.481-484, August 2006.

83. **P. K. Meher**, T. Srikanthan and J. C. Patra, 'Scalable and Modular Memory-Based Systolic Architectures for Discrete Hartley Transform,' *IEEE Transactions on Circuits & Systems-I: Regular Papers*, vol.53, no.5, pp.1065-1077, May 2006.

84. **P. K. Meher**, 'Design of a Fully-Pipelined Systolic Array for Flexible Transposition-Free VLSI of 2-D DFT,' *IEEE Transactions on Circuits & Systems-II: Express Briefs*, vol.52, no.2, pp.85-89, February 2005.

85. N. Sriskanthan, **P. K. Meher**, G. S. Ng, and C. K. Heng, 'A WAP-Teletext System,' *IEEE Transactions on Consumer Electronics*, vol.50, no.1, pp.130-138, January 2004.

86. S. S. Nayak and **P. K. Meher**, 'High-Throughput VLSI Implementation of Discrete Orthogonal Transforms Using Bit-Level Vector-Matrix Multiplier,' *IEEE Transactions on Circuits & Systems-II: Analog & Digital Signal Processing*, vol.46, no.5, pp.655-658, May 1999.

87. **P. K. Meher** and G. Panda, 'Unconstrained Hartley-Domain Least Mean Square Adaptive Filter,' *IEEE Transactions on Circuits & Systems-II: Analog & Digital Signal Processing*, vol.40, no.9, pp.582-585, September 1993.

88. B. K. Mohanty and **P. K. Meher**, 'Area-Delay-Power-Efficient Architecture for Folded Two Dimensional Discrete Wavelet Transform by Multiple Lifting Computation,' *IET Image Processing*, vol.8, no.6, pp.345-353, June 2014.

89. Maher Jridi, **P. K. Meher**, and A. F. Ayman, 'A Zero Quantized DCT Coefficients Prediction Technique for Intra-Frame Video Encoding,' *IET Image Processing*, vol.7, no.2, pp.165-173, July 2013.

90. J. C. Patra, M. Juhola, and **P. K. Meher**, 'Intelligent Sensors using Computationally Efficient Chebyshev Neural Networks,' *IET Science, Measurement & Technology*, vol.2, no.2, pp.68-75, March 2008.

91. B. K. Mohanty and **P. K. Meher**, 'High- throughput and Low-latency Implementation of Bit-level Systolic Architecture for 1-D and 2-D Digital Filters,' *IEE Proceedings ∼ Computers and Digital Techniques*, vol.146, no.2, pp.91-99, March 1999.

92. B. K. Mohanty and **P. K. Meher**, 'Cost- Effective Novel Flexible Cell-Level Systolic Architecture for High-Throughput Implementation of 2-D FIR Filters,' *IEE Proceedings ∼ Computers and Digital Techniques*, vol.143, no.6, pp.436-439, November 1996.

93. S. S. Nayak and **P. K. Meher**, 'A 3-Dimensional Systolic Architecture for Parallel VLSI Implementation of the Discrete Cosine Transform,' *IEE Proceedings ∼ Circuits, Devices and Systems*, vol.143, no.5, pp.255-258, October 1996.

94. **P. K. Meher** and G. Panda, 'Novel Recursive Algorithm and Highly Compact Semi-Systolic Architecture for High-Throughput Computation of 2-D DHT,' *Electronics Letters*, vol.29, no-10, pp.883-885, May 1993.

95. **P. K. Meher**, J. K. Satapathy and G. Panda, 'Efficient Systolic Solution for a New Prime-Factor Discrete Hartley Transform Algorithm,' *IEE Proceedings ∼ Circuits, Devices and Systems*, vol.140, no.2, pp.135-139, April 1993.

96. **P. K. Meher**, J. K. Satapathy and G. Panda, 'New High-Speed Prime-Factor Algorithm for Discrete Hartley Transform,' *IEE Proceedings ∼ Radar & Signal Processing*, vol.140, no.1, pp.63-70, February 1993.

97. **P. K. Meher**, J. K. Satapathy and G. Panda, 'Fast Computation of Multidimensional Discrete Hartley Transform,' *Electronics Letters*, vol.28, no.12, pp.1077-1078, June 1992.

98. G Ganesh Kumar, S. K. Sahoo; **P. K. Meher**, '50 Years of FFT Algorithms and Applications,' *Journal of Circuits, Systems & Signal Processing* (CSSP),vol.38, no.12, pp.5665-5698, December 2019.

99. **P. K. Meher** and S. Y. Park,'Design of Cascaded CORDIC Based on Precise Analysis of Critical Path,' *Electronics*, vol.8, no.4, http://www.mdpi.com/journal/electronics, March 2019.

100. B. K. Meher and **P. K. Meher**,'Analysis of Systolic Penalties and Design of Efficient Digit-Level

Systolic-like Multiplier for Binary Extension Fields,' *Journal of Circuits, Systems & Signal Processing* (CSSP), vol.38, no.2, pp.774-790, February 2019.

101. Syed Naveen Altaf Ahmed **P. K. Meher**, and Vinod A Prasad 'Efficient Cross-Correlation Algorithm and Architecture for Robust Synchronization in Frame-based Communication Systems,' *Journal of Circuits, Systems & Signal Processing* (CSSP), vol.37, no.6, pp.2548-2573, June 2018.

102. Maher Jridi, Ayman Alfalou, and **P. K. Meher**, 'Efficient Approximate Core Transform and its Reconfigurable Architectures for HEVC,' *Journal of Real-Time Image Processing*, (Published Online: 11 April 2018, https://doi.org/10.1007/s11554-018-0768-x).

103. S. Y. Park and **P. K. Meher**, 'Reconfigurable FIR Filter for Dynamic Variation of Filter Order and Filter Coefficients,' *Journal of Semiconductor Technology and Science* (JSTS), vol.16, no.3, pp.261-273, June, 2016.

104. B. K. Mohanty, **P. K. Meher**, S. K. Singhal, and M.N.S. Swamy, 'A High-Performance VLSI Architecture for Reconfigurable FIR using Distributed Arithmetic,' *Integration, the VLSI Journal* (Elsevier), vol.54, no.1, pp.37-46, February 2016.

105. **P. K. Meher**, 'Seamless Pipelining of DSP Circuits,' *Journal of Circuits, Systems & Signal Processing* (CSSP), vol.35, no.4, pp.1147-1162, April 2016.

106. S. Prattipati, M. N. S. Swamy, and **P. K. Meher**, 'A Comparison of Integer Cosine and Tchebichef Transforms for Image Compression using Variable Quantization,' *Journal of Signal & Information Processing* (JSIP), vol.6, pp.203-216, (Published Online: August 2015).

107. B. K. Meher and **P. K. Meher**, 'An Efficient Look-Up Table-Based Approach for Multiplication over GF(2^m) Generated by Trinomials,' *Circuits, Systems & Signal Processing* (Springer), vol.32, no.6, pp.2623-2638, December 2013.

108. Maher Jridi, A. F. Ayman, and **P. K. Meher**, 'Optimized Architecture using a Novel Sub-expression Elimination on Loeffler Algorithm for DCT-Based Image Compression,' *Special Issue on 'VLSI Circuits, Systems, and Architectures for Advanced Image and Video Compression Standards' of VLSI Design*, vol.2012, Article ID 209208. www.hind-awi.com/journals/vlsi/2012/209208/ref/.

109. F. Garcia-Herrero, J. Valls and **P. K. Meher**, 'High Speed RS(255,239) Decoder Based on LCC Decoding,' *Circuits, Systems & Signal Processing* (Springer), vol.30, no.6, pp.1643-1669, October 2011.

110. C-Y Lee and **P. K. Meher**, 'Efficient Bit-Parallel Multipliers over Finite Fields GF(2^m),' *Computers & Electrical Engineering* (Elsevier), vol.36, no.5, pp.955-968, September 2010.

111. A. P. Vinod, E. Lai, D. Maskell, **P. K. Meher**, 'An Improved Common Sub-expression Elimination Method for Reducing Logic Operators in FIR Filter Implementations Without Increasing Logic Depth,' *Integration, the VLSI Journal* (Elsevier), vol.43, no.1, pp.124-135, January 2010.

112. **P. K. Meher**, J. C. Patra and A. P. Vinod, 'Efficient Systolic Designs for 1- and 2-Dimensional DFT of General Transform-Lengths for High-Speed Wireless Communication Applications,' *Journal of Signal Processing Systems* (Springer), vol.60, no.1, pp.1-14, January 2010.

113. J. C. Patra, **P. K. Meher**, and G. Chakraborty, 'Nonlinear Channel Equalization for Wireless Communication Systems using Legendre Neural Networks,' *Signal Processing* (Elsevier), vol.89, no.11, pp.2251-2262, November 2009.

114. T. V. Nguyen, J. C. Patra, and **P. K. Meher**, 'WMicaD: A New Digital Watermarking Technique Using Independent Component Analysis,' *EURASIP Journal on Advances in Signal Processing*, vol.2008,

available online at http://www.hindawi.com, 2008.

115. G. S. Maharana and **P. K. Meher**, 'Algorithm for Efficient Interpolation of Real-Valued Signals using Discrete Hartley Transform,' *Computers & Electrical Engineering* (Elsevier), vol.23, no.3, pp.129-134, 1997.

116. G. S. Maharana, **P. K. Meher**, and B. K. Mohanty, 'Efficient Systolic Architecture for VLSI Realization of 2-D Hartley-Like Transform,' *International Journal of Computer & Applications*, vol.35, no 1, January 2013.

117. J. K. Meher, M.R. Panigrahi, G.N. Dash, **P. K. Meher**, 'Wavelet Based Lossless DNA Sequence Compression for Faster Detection of Eukaryotic Protein Coding Regions,' *International Journal of Image, Graphics & Signal Processing*, vol.4, no 7, pp.47-53, July 2012.

118. J. K. Meher, **P. K. Meher**, G. N. Dash, and M. K. Raval, 'New Encoded Single-indicator Sequences Based on Physico-Chemical Parameters for Efficient Exon Identification,' *International Journal of Bioinformatics Research and Applications*, vol.8, no 2, pp.126-140, March 2012.

119. J. K. Meher, M. K. Raval, **P. K. Meher**, and G. N. Dash, 'The Role of Combined OSR and SDF Method for Pre-Processing of Microarray Data that Accounts for Effective Denoising and Quantification,' *Journal of Signal and Information Processing*, vol.2, no.3, pp.190-195, August 2011.

120. J. K. Meher, G. N. Dash, **P. K. Meher**, and M. K. Raval, 'A Reduced Computational Load Protein Coding Predictor Using Equivalent Amino Acid Sequence of DNA String with Period-3 Based Time and Frequency Domain Analysis,' *American Journal of Molecular Biology Applications*, pp.79-86, July 2011.

121. J. K. Meher, **P. K. Meher**, and G. N. Dash, 'Improved Comb Filter based Approach for Effective Prediction of Protein Coding Regions in DNA Sequences,' *Journal of Signal and Information Processing*, vol.2, no.2, pp.88-99, May 2011.

122. **P. K. Meher** and C-Y. Lee, 'Efficient Designs for AOP-Based Field Multiplication over GF(2^m),' *Journal of Computers*, vol.22, no.3, pp.3-10, October 2011.

123. C-Y. Lee, **P. K. Meher** and Y-H. Chen, 'Error-Correcting Codes for Concurrent Error Correction in Bit-parallel Systolic and Scalable Multipliers for Shifted Dual Basis of GF(2^m),' *Journal of Computers*, vol.22, no.3, pp.37-52, October 2011.

124. C-Y. Lee, **P. K. Meher**, and C-C. Fan, 'Fault-Tolerant Bit-Parallel Multiplier for Polynomial Basis of GF(2^m),' *Journal of Electronic Science and Technology*, vol.7, no.4, pp. 343- 347, December 2009.

125. G. S. Maharana and **P. K. Meher**, 'Parallel Algorithms and Systolic Architectures for 1- and 2-D Interpolation using Discrete Hartley Transform,' *International Journal of Computer & Applications*, vol.22, no.1, pp.1-7, 2000.

126. A. K. Rath and **P. K. Meher**, 'A Novel Reconfigurable Execution Core for Merged DSP Microcontroller,' *Journal of Computer Science*, vol.3, no.10, pp.803-809, 2007.

127. A. K. Rath and **P. K. Meher**, 'Design of a Merged-DSP Microcontroller for Embedded Systems using Discrete Orthogonal Transform,' *Journal of Computer Science*, vol.2, no.5, pp.388-394, 2006.

128. P. K. Behera and **P. K. Meher**, 'A Group-based Ad hoc Network and its Advantages,' *Journal of Computer Science and Informatics*, vol.33, no.1, July-September 2003.

129. S. S. Nayak, and **P. K. Meher**, 'Efficient Systolic Architecture of 2-D Discrete Cosine Transform,' *IETE Journal of Research*, vol.47, no 3 and 4, pp.173-178, May-Aug 2001.

130. A. K. Rath and **P. K. Meher**, 'Embedded System Design: Current Issues and Perspectives,' *Journal of Computer Science and Informatics*, vol.31, no 4, pp.8-18, 2001.

131. B. K. Mohanty and **P. K. Meher**, 'Novel Flexible Systolic Mesh Architecture for Parallel VLSI Implementation of Finite Digital Convolution,' *IETE Journal of Research*, vol.44, no.6. pp.261-266, November-December 1998.

132. **P. K. Meher** and S. K. Pradhan, 'Single Layer Block Neural Network for Solution of Lyapunov Equation,' *IETE Journal of Research*, vol.43, no.5, pp.339 -344, Sep-Oct 1997.

133. G. S. Maharana and **P. K. Meher**, 'Interpolation of 2-D signals using 2-D Hartley-like Transform,' *IETE Journal of Research*, vol.43, no.4, pp.333-335, July-August, 1997.

134. **P. K. Meher** and G. Panda, 'Fast Computation of Circular Convolution of Real-Valued Data Using Prime-Factor Fast Hartley Transform Algorithm,' *Journal of IETE*, vol.41, no.4, pp.261-264, July-August, 1995.

(D) Conference Papers

1. S. S. Wadkar, B. P. Das, and **P. K. Meher**, 'Low Latency Scaling-Free Pipeline CORDIC Architecture Using Augmented Taylor Series,' *The IEEE International Symposium on Smart Electronic Systems* (ISES'19), Rourkela, India, December 16-18, 2019.

2. Dwaipayan Ray, Nithin George, and **P. K. Meher**, 'Analysis and Design of Approximate Inner-Product Architectures Based on Distributed Arithmetic,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'19), Sapporo, Japan, May 26-29, 2019.

3. J. Xie, C-Y Lee, and **P. K. Meher**, 'Low-Complexity Systolic Multiplier for $GF(2^m)$ using Toeplitz Matrix-Vector Product Method,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'19), Sapporo, Japan, May 26-29, 2019.

4. Hadi Ezaldeen, **P. K. Meher**, Rachita Misra, and Ammar Alnahhas , 'Using Machine Learning to Deduce Student Model in E-Learning Systems,' First International Conference on Range Technology (ICORT 2019), February, 15-17, 2019, Integrated Test Range (DRDO) Chandipur, India.

5. Syed Naveen Altaf Ahmed, **P. K. Meher**, and A. P. Vinod, 'An Efficient Spectrum Sensing Technique for Burst Signals Detection Based on Correlation and FFT,'*TENCON 2017*, pp.684-688, Penang, Malaysia, 05-08 November 2017.

6. Syed Naveen Altaf Ahmed, **P. K. Meher**, and A. P. Vinod, 'Fast Acquisition and Time Synchronization of Frequency Hopping Burst Signals,' *International Conference on Signals and Systems 2017* (ICSigSys 2017), Bali, Indonesia, 16-18 May 2017.

7. B. K. Mohanty, **P. K. Meher**, and T. Srikanthan, 'Critical-Path Optimization for Efficient Hardware Realization of Lifting and Flipping DWTs,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'15), pp. 966-969, Lisbon, Portugal, May 24-27, 2015.

8. Xin Lou, **P. K. Meher**, and, Ya Jun Yu, 'Fine-grained Pipelining for Multiple Constant Multiplications,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'15), pp. 1186-1189, Lisbon, Portugal, May 24-27, 2015.

9. C-Y. Lee, and **P. K. Meher**, 'Efficient Subquadratic Parallel Multiplier Based on Modified SPB of $GF(2^m)$,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'15), pp. 1430-1433, Lisbon, Portugal, May 24-27, 2015.

10. C-Y. Lee, **P. K. Meher** and W-Y. Lee, 'Sub-quadratic Space Complexity Digit-Serial Multiplier over Binary Extension Fields using Toom-Cook Algorithm,' *2014 International Symposium on Integrated Circuits* (ISIC), pp. 176-179, Singapore, 10-12 December, 2014.

11. **P. K. Meher**, B. K. Mohanty, and M.N.S Swamy, 'Low-Area and Low-Power Reconfigurable Architecture for Convolution-Based 1-D DWT using 9/7 and 5/3 Filters,' *28th International Conference on VLSI Design* (VLSI 2015), pp. 327-332, Bengaluru, Karnataka, India, 3-7 January, 2015.

12. **P. K. Meher** and S. Y. Park, 'A Novel DA Based Architecture for Efficient Computation of Inner-Product of Variable Vectors,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'14), pp. 369-372, Melbourne, Australia, 1-5 June, 2014.

13. **P. K. Meher**, B. K. Mohanty, and T. Srikanthan, 'Area-Delay Efficient Architecture for MP Algorithm Using Reconfigurable Inner-Product Circuits,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'14), pp. 1308-1311, Melbourne, Australia, 1-5 June, 2014.

14. S. Aggarwal and **P. K. Meher**, 'Reconfigurable CORDIC Architectures for Multi-Mode and Multi-Trajectory Operations,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'14), pp. 2490-2494, Melbourne, Australia, 1-5 June, 2014.

15. Xin Lou, Ya Jun Yu, and **P. K. Meher**, 'High-Speed Multiplier Block Design Based on Bit-Level Critical Path Optimization,' *The IEEE International Symposium on Circuits and Systems* (ISCAS'14), pp. 1308-1311, Melbourne, Australia, 1-5 June, 2014.

16. S. Prattipati, M. N. S. Swamy and **P. K. Meher**, 'A Variable Quantization technique for image compression using Integer Tchebichef Transform,' (Invited Paper), *The Ninth International Conference on Information, Communications and Signal Processing* (ICICS-2013), Tainan, Taiwan, December 2013.

17. S. Prattipati, S. Iswar, M. N. S. Swamy and **P. K. Meher**, 'A Fast 8×8 Integer Tchebichef Transform Implementation and Comparison with Integer Cosine Transform for Image Compression,' *IEEE 56th International Midwest Symposium on Circuits and Systems* (MWSCAS-2013), Columbus, OH, USA, August 2013.

18. S. Y. Park and **P. K. Meher**, 'Flexible Integer DCT Architectures for HEVC,' *IEEE International Symposium on Circuits and Systems* (ISCAS 2013), pp.1376-1379, Beijing, China, May, 2013.

19. Syed Naveen Altaf Ahmed, **P. K. Meher**, and A P Vinod, 'A Low-Complexity Spectrum Sensing Technique for Cognitive Radios Based on Correlation of Intra-Segment Decimated Vectors,' *IEEE International Conference on Communication Systems* (ICCS), pp.443-447, Singapore, November, 2012.

20. Jiafeng Xie, **P. K. Meher**, and Jianjun He, 'Low-Latency Area-Delay-Efficient Systolic Multiplier Over GF(2^m) for a Wider Class of Trinomials using Parallel Register Sharing,' *IEEE International Symposium on Circuits and Systems* (ISCAS 2012), pp.89-92, Seoul, Korea, May, 2012.

21. B. K. Mohanty and **P. K. Meher**, and S. Singhal, 'Efficient Architectures for VLSI Implementation of 2-D Discrete Hadamard Transform,' *IEEE International Symposium on Circuits and Systems* (ISCAS 2012), pp.1480-1483, Seoul, Korea, May, 2012.

22. B. K. Meher and **P. K. Meher**, 'A New Look-Up Table Approach for High-Speed Finite Field Multiplication,' *International Symposium on Electronic System Design* (ISED-2011), pp.51-55, Kochi, India, December, 2011.

23. **P. K. Meher** and S. Y. Park, 'High-Throughput Pipelined Realization of Adaptive FIR Filter Based on Distributed Arithmetic,' *The IEEE/IFIP International Conference on VLSI and System-on-Chip*

(VLSI-SoC 2011), pp.428-433, Hong Kong, China, October 2011.

24. **P. K. Meher** and Y. Pan, 'MCM-Based Implementation of Block FIR Filters for High-Speed and Low-Power Applications,' *The IEEE/IFIP International Conference on VLSI and System-on-Chip* (VLSI-SoC 2011), pp.118-121, Hong Kong, China, October, 2011.

25. **P. K. Meher** and S. Y. Park, 'Low Adaptation-Delay LMS Adaptive Filter Part-I: Introducing a Novel Multiplication Cell,' (Invited Paper) *The 54th IEEE International Midwest Symposium on Circuits and Systems* (MWSCAS 2011), Seoul, Korea, August 2011.

26. **P. K. Meher** and S. Y. Park, 'Low Adaptation-Delay LMS Adaptive Filter Part-II: An Optimized Architecture,' (Invited Paper) *The 54th IEEE International Midwest Symposium on Circuits and Systems* (MWSCAS 2011), Seoul, Korea, August 2011.

27. C-Y. Lee and **P. K. Meher**, 'Speeding up Subquadratic Finite Field Multiplier over GF(2^m) Generated by Trinomials using Toeplitz Matrix-Vector with Inner Product Formula,'*The Fifth International Conference on Genetic and Evolutionary Computing* (ICGEC 2011), Kinmen, Taiwan, August-September 2011.

28. **P. K. Meher** and M. Maheshwari, 'A High-Speed FIR Adaptive Filter Architecture Using a Modified Delayed LMS Algorithm,' *IEEE International Symposium on Circuits and Systems* (ISCAS 2011), pp.121-124, Rio de Janeiro, Brazil, May 2011.

29. Y. Pan and **P. K. Meher**, 'Efficient Coefficient Partitioning for Decomposed DA-Based Inner-Product Computation,' *IEEE International Symposium on Circuits and Systems* (ISCAS 2011), pp.406-409, Rio de Janeiro, Brazil, May 2011.

30. T-B. Juang, **P. K. Meher**, and K-S. Jan, 'High-Performance Logarithmic Converters Using Novel Two-Region Bit-Level Manipulation Schemes,' *The 2011 International Symposium on VLSI Design, Automation and Test,* (VLSI-DAT 2011), pp.390-393, Hsinchu, Taiwan, April 25-27, 2011.

31. T-B. Juang, **P. K. Meher**, and C-C. Chiu, 'Efficient Weighted Modulo $2^n + 1$ Adders by Partitioned Parallel-Prefix Computation and Enhanced Circular Carry Generation,' *The 2011 International Symposium on VLSI Design, Automation and Test,* (VLSI-DAT 2011), pp.402-405, Hsinchu, Taiwan, April 2011.

32. **P. K. Meher**, 'LUT-based circuits for future wireless systems,' (Invited Paper) *The 53rd IEEE International Midwest Symposium on Circuits and Systems,* (MWSCAS 2010), pp.696-699, Seattle, Washington, August 2010.

33. **P. K. Meher**, 'An Optimized Lookup-Table for the Evaluation of Sigmoid Function for Artificial Neural Networks' *The18th IEEE/IFIP International Conference on VLSI and System-on-Chip,* (VLSI-SoC 2010), pp.91-95, Madrid, Spain, September 2010.

34. **P. K. Meher**, 'Novel Input Coding Technique for High-Precision LUT-Based Multiplication for DSP Applications' *The18th IEEE/IFIP International Conference on VLSI and System-on-Chip,* (VLSI-SoC 2010), pp.201-206, Madrid, Spain, September 2010.

35. **P. K. Meher**, 'Efficient Designs for Memory-Based Computation of Inner-Product for Digital Signal Processing Applications,' *International Symposium on Electronic System Design,* (ISED-2010), pp.95-100, Bhubaneswar, India, December 2010.

36. **P. K. Meher**, S-F. Hsiao, M-Y. Tsai, and C-S. Wen 'Low-Cost Design of Serial-Parallel Multipliers Over GF(2^m) Using Hybrid Pass-Transistor Logic (PTL) and CMOS Logic,' *International Symposium on Electronic System Design,* (ISED-2010), pp.131-134, Bhubaneswar, India, December 2010.

37. T-B. Juang, **P. K. Meher**, and C-C. Kuan, 'Area-Efficient Parallel-Prefix Ling Adders,' *IEEE Asia Pacific Conference on Circuits and Systems,* (APCAS 2010) Kuala Lumpur, Malaysia, December 2010.

38. J. C. Patra, N. V. Georgel, and **P. K. Meher**,' DNA Microarray Analysis Using Equalized Orthogonal Mapping,' *International Joint Conference on Neural Networks,* (IJCNN 2010), Barcelona, Spain, July 2010.

39. J. C. Patra, J. Abraham, **P. K. Meher**, and G.C. Chakraborty' An Improved SOM-based Visualization Technique for DNA Microarray Data Analysis,' *International Joint Conference on Neural Networks,* (IJCNN 2010), Barcelona, Spain, July 2010.

40. **P. K. Meher**, Y. Ha and C-Y Lee, 'An Optimized Design of Serial-Parallel Finite Field Multiplier for GF(2^m) Based on All-One Polynomials,' *The 14th Asia and South Pacific Design Automation Conference,* (ASP-DAC 2009), pp.210-215, Japan, January 2009.

41. **P. K. Meher**, 'New Approach to LUT Implementation and Accumulation for Memory-Based Multiplication,' *IEEE International Symposium on Circuits and Systems,* (ISCAS'09), pp.453-456, Taipei, Taiwan, May 2009.

42. **P. K. Meher** and C-Y Lee, 'Scalable Serial-Parallel Multiplier over GF(2^m) by Hierarchical Pre-Reduction and Input Decomposition,' *IEEE International Symposium on Circuits and Systems,* (ISCAS'09), pp.2910-2913, Taipei, Taiwan, May 2009.

43. **P. K. Meher**, 'New Look-up-table Optimizations for Memory-based Multiplication,' *International Symposium on Integrated Circuits,*, pp.663-666, Singapore, December 2009.

44. B. K. Mohanty and **P. K. Meher**, 'Bit-serial Systolic Architecture for 2-D Non-separable Discrete Wavelet Transform,' *12th International Symposium on Integrated Circuits,* (ISIC 2009) pp.159-162, Singapore, December 2009.

45. B. K. Mohanty and **P. K. Meher**, 'Efficient Multiplierless Designs for 1-D DWT using 9/7 Filters based on Distributed Arithmetic,' *12th International Symposium on Integrated Circuits,* (ISIC 2009), pp.364-367, December 2009.

46. J. K. Meher, **P. K. Meher**, and G. N. Dash, 'Comb Filter Based Approach for Prediction of Protein Coding Region,' *International Conference on Electronic Design and Signal Processing,* (ICEDSP2009), Manipal, India, December 2009.

47. **P. K. Meher**, 'The Look-up-Table Based Computing Systems: Applications and Current Perspectives,' *The 3rd Asia-Pacific Embedded Systems Education and Research Conference,* (APESER 2009), Singapore, December 2009.

48. C-Y Lee and **P. K. Meher**, 'Fault Tolerant Dual Basis Multiplier Over GF(2^m),' *2009 IEEE Circuits and Systems International Conference on Testing and Diagnosis,* (ICTD'09), Chengdu, China, April 2009.

49. C-Y Lee and **P. K. Meher**, 'Fault-Tolerant Bit-Parallel Multiplier for Polynomial Basis of GF(2^m),' *2009 IEEE Circuits and Systems International Conference on Testing and Diagnosis,* (ICTD'09), Chengdu, China, April 2009.

50. J. C. Patra, N. C. Thanh, and **P. K. Meher**,' Computationally Efficient FLANN-based Intelligent Stock Price Prediction System,' *International Joint Conference on Neural Networks,* (IJCNN 2009), pp.2431-2438, Atlanta, June 2009.

51. J. C. Patra, C. Bornand, and **P. K. Meher**, 'Laguerre Neural Network-Based Smart Sensors for Wireless Sensor Networks,' *IEEE Instrumentation and Measurement Technology Conference,* (I2MTC '09), pp.832-837, Singapore, May 2009.

52. B. K. Mohanty and **P. K. Meher**, 'New Scan Method and Pipeline Architecture for VLSI Implementation of Separable 2-D FIR Filters Without Using Transposition,' *IEEE International Region 10 Conference,* (TENCON' 08), Hyderabad, India, November 2008.

53. B. K. Mohanty and **P. K. Meher**, 'Delayed Block LMS Algorithm and Concurrent Architecture for High-Speed Implementation of Adaptive FIR Filters,' *IEEE International Region 10 Conference,* (TENCON' 08), Hyderabad, India, November 2008.

54. J. C. Patra, W. C Chin, **P. K. Meher** and G. Chakraborty,' Legendre-FLANN-based Nonlinear Channel Equalization in Wireless Communication System,' *IEEE International Conference on Systems, Man and Cybernetics,* (SMC 2008), pp.1826-1831, Singapore, October 2008.

55. J. C. Patra, **P. K. Meher** and G. Chakraborty,'Development Of Intelligent Sensors using Legendre Functional-Link Artificial Neural Networks,' *IEEE International Conference on Systems, Man and Cybernetics,* (SMC 2008), pp.1140-1145, Singapore, October 2008.

56. J. C. Patra, A. Karthik, **P. K. Meher** and C. Bornand,' Robust CRT-Based Watermarking Technique for Authentication of Image and Document,' *IEEE International Conference on Systems, Man and Cybernetics,* (SMC 2008), pp.3250-3255, Singapore, October 2008.

57. J. C. Patra, S. Sood, **P. K. Meher** and C. Bornand,' Content-Based Image Retrieval using Orthogonal Moments Heuristically,' *IEEE International Conference on Systems, Man and Cybernetics,* (SMC 2008), pp.512-517, Singapore, October 2008.

58. C-Y Lee and **P. K. Meher**, 'Efficient Bit-Parallel Multipliers in Composite Fields,' *IEEE Asia-Pacific Services Computing Conference,* (APSCC 2008), pp.686-691, Yilan, Taiwan, December 2008.

59. S. Natarajan, A.R. Mohan, and **P. K. Meher**, 'Systolic array realization of a neural network-based face recognition system,' *IEEE International Conference on Industrial Electronics and Applications,* (ICIE'08), pp.1864-1869, Singapore, June 2008.

60. S. Natarajan, A.R. Mohan, and **P. K. Meher**, 'An Embedded Face Recognition System on A VLSI Array Architecture and its FPGA Implementation,' *34th Annual Conference of IEEE Industrial Electronics,* (IECON'08), pp.2432-2437, Singapore, June 2008.

61. **P. K. Meher**, 'Efficient Systolization of Cyclic Convolution for Systolic Implementation of Sinusoidal Transforms,' *IEEE International Conference on Application-specific Systems, Architectures and Processors* (ASAP'08), pp.97-101, Leuven, Belgium, July 2008.

62. **P. K. Meher** and J. C. Patra, 'Fully-Pipelined Efficient Architectures for FPGA Realization of Discrete Hadamard Transform,' *IEEE International Conference on Application-specific Systems, Architectures and Processors* (ASAP'08), pp.43-48 Leuven, Belgium, July 2008.

63. B. K. Mohanty and **P. K. Meher**, 'Throughput-Scalable Hybrid-Pipeline Architecture for Multilevel Lifting 2-D DWT Of JPEG 2000 Coder,' *IEEE International Conference on Application-specific Systems, Architectures and Processors* (ASAP'08), pp.311-315, Leuven, Belgium, July 2008.

64. B. K. Mohanty and **P. K. Meher**, 'Concurrent Systolic Architecture for High-Throughput Implementation of 3-Dimensional DWT,' *IEEE International Conference on Application-specific Systems, Architectures and Processors* (ASAP'08), pp.168-172, Leuven, Belgium, July 2008.

65. S. Ishwar, **P. K. Meher**, and M. N. S. Swamy, 'Discrete Tchebichef Transform-a Fast 4x4 Algorithm and its Application in H.264/AVC,' *IEEE International Symposium on Circuits and Systems* (ISSCAS'08), pp.260-263, May 2008.

66. P. Sinha, M. N. S. Swamy, and **P. K. Meher**, ' Fully-Pipelined CORDIC Implementation of Subspace-Based Speech Enhancement,' *The 50th IEEE International Midwest Symposium on Circuits and Systems,* MWSCAS'07, pp.97- 100, Montreal, Canada, August 2007.

67. B. K. Mohanty and **P. K. Meher**, 'Bit-Serial Systolic Architecture for 2-D Non-Separable Discrete Wavelet Transform,' *International Conference on Intelligent & Advanced Systems* (ICIAS 2007), Kualalampur, Malaysia, November 2007.

68. **P. K. Meher**, 'High-Throughput Hardware-Efficient Digit-Serial Architecture for Field Multiplication over GF(2^m),' *The Sixth International Conference on Information, Communications and Signal Processing* (ICICS 2007), December 2007.

69. **P. K. Meher** and J. C. Patra, 'A New Convolutional Formulation of Discrete Cosine Transform for Systolic Implementation,' *The Sixth International Conference on Information, Communications and Signal Processing* (ICICS 2007), December 2007.

70. **P. K. Meher**, 'Low-Latency Hardware-Efficient Memory-Based Design for Large-Order FIR Digital Filters,' *The Sixth International Conference on Information, Communications and Signal Processing* (ICICS 2007), December 2007.

71. **P. K. Meher**, 'Memory-Based Hardware for Resource-Constraint Digital Signal Processing Systems,' *the Sixth International Conference on Information, Communications and Signal Processing* (ICICS 2007), December 2007.

72. J. C. Patra, A. Devi, and **P. K. Meher**, 'Radial Basis Function Implementation of Intelligent Pressure Sensor on Field Programmable Gate Array,' *The Sixth International Conference on Information, Communications and Signal Processing* (ICICS 2007), December 2007.

73. J. C. Patra, S. Detpongsante, **P. K. Meher**, and Ee Luang Ang, 'Equalized Orthogonal Map-based DNA Microarray Data Analysis for Cancer Diagnosis,' *Sixth International Conference on Information, Communications and Signal Processing* (ICICS 2007), December 2007.

74. **P. K. Meher**, 'Efficient Systolization of Cyclic Convolutions Using Low-Complexity Rectangular Transform Algorithms,' *IEEE International Symposium on Signals, Circuits and Systems* (ISSCS 2007), pp.189-192, July, 2007.

75. **P. K. Meher**, J. C. Patra, and A. P. Vinod, 'Novel Recursive Solution for Area-Time Efficient Systolization of Discrete Fourier Transform,' *IEEE International Symposium on Signals, Circuits and Systems* (ISSCS 2007), pp.193-196, July, 2007.

76. B. K. Mohanty and **P. K. Meher**, 'Pipelined Architecture for High-Speed Implementation of Multilevel Lifting 2-D DWT using 9/7 Filters,' *IEEE International Symposium on Signals, Circuits and Systems* (ISSCS 2007), pp.137-140, July, 2007.

77. G. Deepak, **P. K. Meher**, and A. Sluzek, 'Performance Characteristics of Parallel and Pipelined Implementation of FIR Filters in FPGA Platform,' *IEEE International Symposium on Signals, Circuits and Systems* (ISSCS 2007), pp.245-248, July, 2007.

78. **P. K. Meher**, 'Systolic Formulation for Low-Complexity Serial-Parallel Implementation of Unified Finite Field Multiplication over GF(2m),' *IEEE International Conference on Application-Specific Systems, Architectures and Processors* (ASAP 07), pp.134-139, July 2007.

79. **P. K. Meher** and J. C. Patra, 'A New Approach to Secure Distributed Storage, Sharing and Dissemination of Digital Image,' *IEEE International Symposium on Circuits and Systems* (ISCAS 2006), pp.373-376, Greece, May 2006.

80. **P. K. Meher**, J. C. Patra, and M. R., Meher, 'Low-Complexity Technique for Secure Storage and Sharing of Biomedical Images,' *IEEE International Symposium on Circuits and Systems* (ISCAS 2006), pp.4803-4806, Greece, May 2006.

81. **P. K. Meher**, A. P. Vinod, J. C. Patra and M. N. S. Swamy, 'Reduced- Complexity Concurrent Systolic Implementation of the Discrete Sine Transform,' *IEEE Asia Pacific Conference on Circuits and Systems* (APCCAS 2006), December 2006, pp.1537-1540.

82. **P. K. Meher**, J. C. Patra, and A. P. Vinod, 'A 2-D Systolic Array for High-Throughput Computation of 2-D Discrete Fourier Transform,' *IEEE Asia Pacific Conference on Circuits and Systems* (APCCAS 2006), pp.1927-1930, December 2006.

83. B. K. Mohanty and **P. K. Meher**, 'Systolic Architecture for Transposition-Free VLSI Implementation of 2-D DWT,' *IEEE International Conference on Communication Systems* (ICCS 2006), October-November 2006.

84. B. K. Mohanty and **P. K. Meher**, 'Bi-Layer Systolic Architecture for Bit-Serial Implementation of Discrete Wavelet Transform,' *IEEE International Conference on Communication Systems* (ICCS 2006), October-November 2006.

85. B. K. Mohanty and **P. K. Meher**, 'Merged-Cascaded Systolic Array for VLSI Implementation of Discrete Wavelet Transform,' *IEEE Asia Pacific Conference on Circuits and Systems* (APCCAS 2006), pp.462-465, December 2006.

86. J. C. Patra, H. Y. Lee, **P. K. Meher**, and E. L. Ang, 'Field Programmable Gate Array Implementation of a Neural Network-Based Intelligent Sensor System,' *International Conference on Control Automation Robotics and Vision* (ICCARV 2006), pp.333-337, December 2006.

87. J. C. Patra, W. Soh, E. L. Ang, and **P. K. Meher**, An improved SVD-based watermarking technique for image and document authentication, *IEEE Asia Pacific Conference on Circuits and Systems* (APCCAS 2006), pp.1984-1987, December 2006.

88. B. K. Mohanty and **P. K. Meher**, 'VLSI Architecture for High-Speed / Low-Power Implementation of Multilevel Lifting DWT,' *IEEE Asia Pacific Conference on Circuits and Systems* (APCCAS 2006), pp.458- 461, December 2006.

89. A. P. Vinod, C-H. Chang, **P. K. Meher**, and A. Singla, 'Low Power FIR Filter Realization Using Minimal Difference Coefficients: Part I-Complexity Analysis,' *IEEE Asia Pacific Conference on Circuits and Systems* (APCCAS 2006), pp.1549-1552, December 2006.

90. P. Vinod, C-H., Chang **P. K. Meher**, and A. Singla, 'Power FIR Filter Realization Using Minimal Difference Coefficients: Part II-Algorithm,' *IEEE Asia Pacific Conference on Circuits and Systems* (APCCAS 2006), pp.1553-1556, December 2006.

91. Zhao Chang, A. P. Vinod, and **P. K. Meher**, 'Reconfigurable Architectures for Low Complexity Software Radio Channelizers using Hybrid Filter Banks,' *The 10th IEEE International Conference on Communication Systems* (ICCS 2006), October 2006.

92. **P. K. Meher** and M. R. Meher, 'A Low Complexity Technique for Data Fusion in Digital Images and Lossless Retrieval,' *The Third International Conference on Intelligent Sensing and Information Processing* (ICISIP 2005), pp.106-109, December 2005.

93. **P. K. Meher**, 'Unified DA-based Parallel Architecture for Computing the DCT and the DST,' *The The Fifth International Conference on Information, Communications & Signal Processing* (ICICS 2005), pp.1278-1282, December, 2005.

94. **P. K. Meher**, 'Area-Time Efficient Systolic Architecture for the DCT,' *The 10th Asia-Pacific Computer Systems Architecture Conference* (ACSAC 2005), *Lecture Notes on Computer Science* (LNCS 3740), pp.787-794, Springer-Verlag, October, 2005.

95. **P. K. Meher**, 'A New Convolutional Formulation of the DFT and Efficient Systolic Implementation,' *IEEE International Region 10 Conference* (TENCON' 05), November, 2005.

96. **P. K. Meher**, T. Srikanthan and J. Gupta, and H. K. Agarwal, 'Low-Complexity Unified-Adaptive Compression of Biomedical Images Using Integer Hartley Transform,' *The First International Bioengineering Conference*, pp.125-128, September 2004.

97. **P. K. Meher**, T. Srikanthan and J. Gupta, and H. K. Agarwal, 'Controlled-Accuracy-Lossy Compression Using Integer Hartley Transform,' *IEEE International Symposium on Consumer Electronics* (ISCE-2003), December 2003 (CD).

98. **P. K. Meher**, T. Srikanthan and J. Gupta, and H. K. Agarwal, 'Near Lossless Image Compression Using Lossless Hartley Like Transform,' *Joint Conference of the 4th International Conference on Information, Communications and Signal Processing, and the Fourth Pacific Rim Conference on Multimedia* (ICICS-PCM 2003), vol.1, pp.213-217, December 2003.

99. **P. K. Meher**, T. Srikanthan and A. K. Rath, 'Design of An Efficient Embedded Merged DSP Microcontroller Using Configurable Cores,' *IEEE International Symposium on Consumer Electronics* (ISCE-2003), December 2003 (CD).

100. J. C. Patra, Ee-L. Ang and **P. K. Meher**, 'Neural Network-based Nonlinear ALE for Detection and Tracking of Dim Targets,' *International Symposium on Intelligent Signal Processing and Communication Systems* (ISPACS-2003), Awaji Island, Japan, pp.213-218, December 2003.

101. N. Sriskanthan, H. C. Khoo and **P. K. Meher**, 'PC-Based TV Text Insertion System,' *IEEE International Symposium on Consumer Electronics* (ISCE-2003), December 2003 (CD).

102. Ganguli, S. Nandi and **P. K. Meher**, 'An Improvement of ODMRP for Reliable Delivery of Busty Traffic,' *IEEE Conference on Convergent Technologies for the Asia-Pacific* (TENCON' 03), vol.3, pp.1067-1071, October 2003.

103. **P. K. Meher** and T. Srikanthan, 'A Scalable Multiplier-less Fully-Pipelined Architecture for VLSI Implementation of the Discrete Hartley Transform,' *IEEE International Symposium on Signals, Circuits and Systems,* (SCS-2003), Iasi, Romania, pp.393-396, July 2003.

104. **P. K. Meher** T. Srikanthan, M. M. Kumar, and S. Arunkumar, 'Low-Power Transform-Domain Coding by Separable Two-Dimensional Hartley-Like Transform,' *International Conference on Embedded Systems and Applications* (ESA-03), Las Vegas, Nevada, USA, pp.228-236, June 2003.

105. A. K. Rath and **P. K. Meher**, 'Re-configurable Execution Core for High-Performance DSP Applications,' *IEEE Asia Pacific Conference on Circuit & System* (APCCAS 2002), vol.2, pp. 509-514, December-2002.

106. P. K. Behera and **P. K. Meher**, 'Effective Communication in Ad hoc Network of Mobile Users' Group,' *IEEE Asia-Pacific Conference on Circuit & System* (APCCAS 2002), vol.2, pp.461-465, December-2002.

107. P. K. Behera and **P. K. Meher**, 'Prospects of Group-based Communication in Mobile Ad hoc Networks,' *International Workshop on Distributed Computing* (IWDC-2002), Kolkata, India, *Lecture Notes on Computer Science* (LNCS 2571), pp.174-183, Springer-Verlag, 2002.

108. P. K. Behera and **P. K. Meher**, 'Security Issues in Mobile Ad hoc Networks,' *The 28th Annual Convention of IEEE India Council*, Kolkata, India, pp.1-4, December 2002.

109. K. Rath and **P. K. Meher**, 'Core-based Design of Embedded DSP System,' *The XXXVII National Convention 2002 of Computer Society of India,* (CSI-2002), Bangalore, India, pp.127-136, October 2002.

110. P. K. Behera and **P. K. Meher**, 'Authenticated Message Passing in Mobile Ad hoc Networks,' *The XXXVII National Convention 2002 of Computer Society of India* (CSI-2002), Bangalore, India, October 2002. http://www.csi-india.org/hmk/Contributed/ 11.doc.

111. A. K. Rath and **P. K. Meher**, 'Merged DSP Microcontroller using Reconfigurable Execution Core,' *4th Asian Control Conference* (ASCC-2002), Singapore, pp.1910-1915, September-2002.

112. P. K. Behera and **P. K. Meher**, 'Group-based Ad hoc Network and its Advantages,' *The 15th International Conference on Computer Communication* (ICCC-2002), Mumbai, India, pp.389-397, August 2002.

113. A. K. Rath and **P. K. Meher**, 'Run-time Re-configurable Execution Core for Digital Signal Processing Applications,' *The 5th International Conference on Information Technology* (CIT-2002), Bhubaneswar, India, pp.315-318, December 2002.

114. P. K. Behera and **P. K. Meher**, 'Implementation of Mobile Users Club for Group-based Communication in Ad hoc Networks,' *The 5th International Conference on Information Technology* (CIT-2002), Bhubaneswar, India, pp.167-173, December 2002.

115. A. K. Rath and **P. K. Meher**, 'Embedded DSP Microcontroller using Discrete Orthogonal Transform,' *The XXXVI Annual Convention of Computer Society of India*, Kolkata, India, pp. C7-C11, November 2001.

116. **P. K. Meher** and S. K. Pradhan, 'Dedicated Architecture for Solution of Linear Systems using Least Mean Square Optimization,' *International Conference on High Performance Computers* (HCP-97), Santiago de Compostela, Spain, July 1997.

117. G. S. Maharana and **P. K. Meher**, 'Fast Algorithm for Interpolation of 2-D Real- Valued Data using 2-D DHT-based Sub-matrices,' *IASTED International Conference on Signal and Image Processing*, New Orleans, Louisiana, USA, December 1997.

118. K. Mohanty and **P. K. Meher**, 'Systolic Arrays for High-Speed Implementation of IIR Digital Filters,' *IASTED International Conference on Signal and Image Processing*, New Orleans, Louisiana, USA, December 1997.

119. **P. K. Meher** and S. K. Pradhan, 'IIR System Modeling Using Artificial Neuron,' *IASTED International Conference on Signal & Image Processing and Applications*, France, June 1996.

120. **P. K. Meher** and S. K. Pradhan, 'Solution of Linear and Equations using Delayed Neuron,' *National Seminar on Theoretical Computer Science* (NSTCS-6), Banasthali Vidyapith, India. August 1996.

121. G. S. Maharana and **P. K. Meher**, 'Efficient Interpolation of 2-D Signals using Hartley-Like Transform,' *IASTED International Conference on Signal and Image Processing,* Orlando, Florida, USA, November 1996.

122. **P. K. Meher** and S. K. Pradhan, 'Optimal Neural Network for Solution of Lyapunov Equation,' *IEEE International Conference on Neural Networks* (ICNN 95), Perth, Western Australia, vol.1, pp.555-559, November 1995.

123. **P. K. Meher**, 'A Systolic Array Architecture for Parallel VLSI Implementation of Linear Convolution,' *Seminar on Super Computing for Scientific Visualization*, Bhaba Atomic Research Centre (BARC), India, pp.413-415, February 1994.

124. **P. K. Meher**, J. K. Satapathy and G. Panda, 'An Efficient Architecture for Parallel VLSI Implementation of Discrete Hartley Transform,' *IEEE Kharagpur Section Tech. Conf, on Application of Parallel and Distributed Processing*, Indian Institute of Technology, Kharagpur, India, pp.11, January 1993.

125. **P. K. Meher** and S. K. Udgata, 'Recovery of Harmonic Components of a Signal Buried in Noise using Artificial Neuron,' *Workshop Cum Symposium on Applications of Neural Networks in Nuclear Science and Industry* (BARC), India, pp.C1.1-C1.8, November, 1993.

126. **P. K. Meher** and S. K. Udgata, 'Adaptive Line Enhancement using and Artificial Neuron,' *Workshop Cum Symposium on Applications of Neural Networks in Nuclear Science and Industry*, (BARC), India, pp.C3.1-3.9, November 1993.

127. **P. K. Meher**, S. K. Udgata and S. K. Pradhan, 'A Novel Approach for Inversion of Non-Singular Matrices using Single Layer Neural Networks,' *Workshop Cum Symposium on Applications of Neural Networks in Nuclear Science and Industry* (BARC), India, pp.F2.1-F2.9, November 1993.